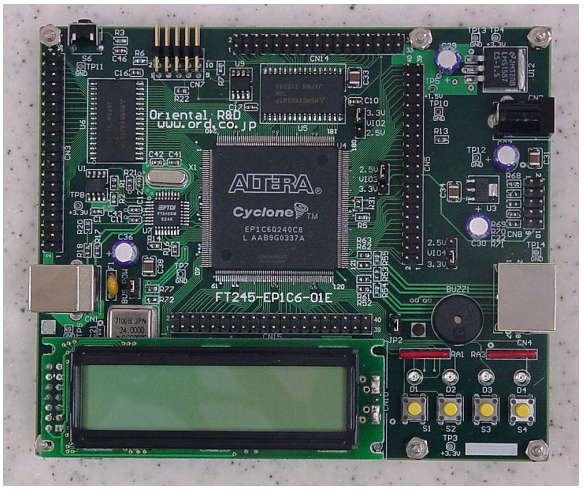
FT245-EP1C6



FT245-EP1C6 Specification

Size: 130 x 110mm
FPGA chip: EP1C6Q240C8
FPGA configuration: AS and JTAG
USB controller: FTDI FT245BM
USB port: Type B
Configuration ROM: EPCS1
RAM: Two 8bit-512K(70ns) SRAM's
User I/O: 5 I/Os in Bank 1, 43 I/Os in Bank 3 and 36 I/Os in Bank4
Operational parts: A 16x2 LCD, 4 push switches, 4 dipswitches, a buzzer and4 LEDs
Clock: A built-in 24MHz crystal and a circuit pattern for user crystal
Power: 5V DC (USB bus power or DC jack)

Development environment

"QuartusII Web Edition" is available at the Altera Web site without charge.
A cable "ByteBlaster II" for down loading is required.

USB device driver

The latest device driver is available from the FTDI Web site at
http://www.ftdichip.com/

FT245-EP1C6

[Altera Cyclone FPGA evaluation board]
[Oriental R & D]

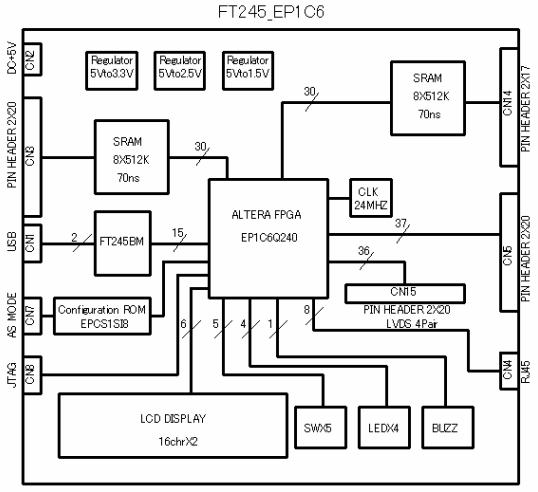
FT245-EP1C6 is an evaluation board that uses an Altera's Cyclone series FPGA and an FTDI's USB controller. FT245-EP1C6 is accompanied with a USB device driver, a control program and an FPGA sample circuit written in Verilog. FT245-EP1C6 enables designers to build PC friendly systems rapidly.

Noteworthy characteristics

I/O banks are driven with 3.3V or 2.5V that the designer defines (the bank 1 and 2 are 3.3V only).

LVDS super speed communications are available via an RJ45 connector.

Since FT245-EPC has two banks of 512K SRAM, the FPGA may access one of the memories while the host PC is accessing the other.



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